Design Rules
For Co-fired
Aluminum Nitride Ceramic
Substrates

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1.0 Introduction

The design rules contained in this document are driven by manufacturing technology and yield considerations. The layout rules, or design conventions, contained in the companion document Layout Rules for Aluminum Nitride Designs are imposed by conventions and tools used for manufacturing data preparation.

Design rules tend to impact the producibility and cost of a product for the life of the product. Layout rules tend to impact the non-recurring engineering cost and time required to obtain correct manufacturing tooling (data) and hence functional prototypes. Both are important!

1.1 Technical Support

For further details on the rules described in this document, contact one of the following people:

- Frank Polese 858-486-8846 fpolese@oasismaterials.com
- Stephen Nootens 858-486-8846 snootens@oasismaterials.com

1.2 Optimizing Rules

The rules in this document represent physical design limits that must be observed however, it is recommended that designs be done as much as possible without pushing to the limits. For example, where spacing permits, lines should be separated by greater than the minimum spacing. Risk sites to be avoided or minimized during design are illustrated in Figure 2.2

1.3 Definitions

Many of the terms and features described below are illustrated in figures in this document or in Layout Rules for Aluminum Nitride Designs.

Via (Via Hole): Hole provided in a dielectric (ceramic) layer which, when filled with conductive paste and sintered, forms an electrical connection vertically between metallization layers.

Via Cap (Capture Pad): Circular pad provided at each via location in a metallization layer to assure that the vias are fully contacted (i.e., captured) during lamination and sintering. A Via Cap must be present on both metallization layers contiguous to a via.

Line: Geometric design entity defined by a set of vertex points and a constant width centered about the centerline connecting two contiguous vertex points.

Line Segment: A single straight section of a line between two neighboring vertex points. Line segments are not separate geometric design entities, except for the case of a single segment line.

Multi-Segment Line: A single geometric feature consisting of a line with two or more line segments (therefore, three or more vertex points).

Line With and Without Ends: "Ends" refer to a method of line construction available in certain design systems. Specifically, when a line is drawn as a "line with ends," then the physical length is automatically extended at both ends by one-half the width of the line. A "line without ends" does not have such extensions (see Layout Rules for Aluminum Nitride Designs). The layout rules only allow the use of square ends; rounded ends are not allowed.
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Trace: A line, or group of connected lines, used to make a wiring net connection as on a Redistribution or Signal Layer. Lines used to create meshes or border or fill lines are not traces.

Grid: A rectilinear network of reference points. See Section 2.1, "Design Grid" on page 6 for details. See also the term "CAD grid" in Layout Rules for Aluminum Nitride Design.

Figure 1.1 – Lines connecting to Via Caps and Via

Mesh Line: A line used to create the mesh pattern for References, Power Distribution, or Mixed Layers.

Border Line: A line used to define the border or outline of a region to be filled in with Fill Lines. Mesh Lines are a type of 8order Line.

Fill Line: A line used to fill in area within a region defined by 8order Lines.

Pitch: This is the distance between the centers of two or more features (in many cases, this coincides with the grid).

Active Area: Refers to the area of the substrate contained within the boundaries of electrically active circuit metal. The active area may include chip C4 or wire bond pads, redistribution and X-Y wiring, capacitor ads, reference plane metallurgy, other circuit wiring and 8SM I/O pads. The active area does not necessarily include fiducials, part numbers, A01 locators, or other metallurgy not electrically connected to other features.

Risk Site: An area in a design where the risk of problems at manufacturing is greater. Risk sites are described further in Section 2.6, "Things to Avoid" on page 11.

Internal Metallization: Metallization (on a metallization layer) that is located internal to a substrate.

External Metallization: Metallization (on a metallization layer) that is on an external surface of a substrate, either on the Top, the Bottom, or in an exposed cavity.

TSM: Top Surface Metallization.
BSM: Bottom Surface Metallization
FDSH: Full Dense Square Hatch
HDSH: Half Dense Square Hatch
SCM: Single Chip Module(s)
MCM: Multi-chip Module(s)
SBC: Solder Ball Carrier
EC: Engineering Change

1.3.1 Layer Types

Most of the common layer types are further defined in their own sections (e.g., Redistribution Layers, etc.)
Basic layer descriptions and some other special layers are described here.

Redistribution Layer: A metallization layer (in a ceramic substrate) that implements the interconnections from chip bond pads to some feature on a Design Grid point.

Signal Layer: A metallization layer on which the features (traces and Via Caps) are laid out following the strict orthogonal routing and Via placement rules.

Reference Layer: A metallization layer that functions primarily to provide a voltage reference for signal traces. Reference layer features are based on Mesh Lines with Fill Lines and Via Caps as required.

Power Distribution Layer: A metallization layer that functions primarily to distribute electrical current and voltage (power). It will typically have a higher metal loading than a Reference Layer.

Mixed Layer: A metallization layer that combines the functions and features of a Redistribution or Signal Layer with a Reference or Power Distribution Layer.

Via Layer: A layer of ceramic in the make-up of a substrate that contains vias.

Dummy Layer: A layer of ceramic on the make-up of a substrate that contains no metallurgy whatsoever. It is used for increasing the overall thickness of the substrate.

Through Via Layer (or Blank Layer): A layer of ceramic in the make-up of a substrate that contains through vias and is used to increase the overall thickness of the substrate or to change the electrical characteristics of the substrate. It will be identical to at least one other via layer.
2.0 Global Layer Rules

The rules in this section apply to all layers, both metallization and via, as appropriate.

In order to improve manufacturing yields and to lower costs, make conservative design choices whenever possible. Do not push the limits of the rules unless necessary to do so in order to implement a given design.

2.1 Design Grid

A design grid is a regular, rectilinear network of design reference points on the plane of a design layer. A design grid as used here is different from a CAD grid as discussed in Layout Rules for Aluminum Nitride Designs, which is typically a finer scale grid. The dimension of the grid is the largest common increment of a repeatable pattern found in the elements of the design. Example: Feature A is being placed every 0.750 mm and Feature B is being placed every 0.500 mm. The design grid dimension here would be 0.250 mm.

Design grids are highly recommended. Substrate designs will typically benefit substantially from use of a design grid. The lack of a judiciously chosen design grid could render effectively not manufacturable.

It is particularly important that most or all vias be placed on a common grid of ≥225 l/m, especially in designs containing many vias. This allows faster via punching during fabrication and thus lower costs. Wire bond pads and other special features may force some vias to be placed off this primary grid, but such instances should be minimized.

All vias not on the primary grid should be on a secondary to tertiary grid as necessary.

2.2 Metallization Layers

2.2.1 Metal Patterning

The design rules in this document are for a manufacturing process that uses a screened metal patterning technique. A second technique that can provide thicker metallization patterns, and hence lower resistivity, is available; however, this “thicker” process carries substantial restrictions on the feature “patterns” that can be implemented as indicated in Table 1. Customers interested in the thicker metallization should contact Technical Support (Section 1.1).

<table>
<thead>
<tr>
<th>Technique</th>
<th>Screened</th>
<th>Thicker</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Restrictions</td>
<td>Few</td>
<td>Many (Technical Support required)</td>
</tr>
<tr>
<td>Metallization Thickness</td>
<td>Thinner (15 l/m)</td>
<td>Thicker (-2x)</td>
</tr>
<tr>
<td>Sheet Resistance</td>
<td>Higher (-2x)</td>
<td>Lower</td>
</tr>
</tbody>
</table>

The nominal thickness of screened metallization is 15 l/m as indicated in Table 1. Metal features have a sloped rather than vertical edge profile. Contact Technical Support (Section 1.1) for more information on metallization.
2.2.2 Metal Loading

Metal loading refers to the spatial distribution of metal features in a co-fired ceramic body. Two kinds of loading are important:

- Transverse Loading on individual layers
- Z-Loading, the loading on all layers form top-to-bottom of the substrate

Metal loading affects the spatial distortion created in a ceramic body during sintering due to slight differential shrinkage between metal and ceramic. Minimizing the amount of, and variations in the distribution of, metal helps to control this distortion. Table 2 indicates the maximum layer loadings.

Table 2 - Maximum Layer Loadings

<table>
<thead>
<tr>
<th>Layer Type</th>
<th>Recommended/Standard</th>
<th>Enhanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>All Layers</td>
<td>40%</td>
<td>50%</td>
</tr>
</tbody>
</table>

Contact Technical Support to discuss higher Layer Loading.

Different metal pastes are used as a function of metal loading. Pastes used to allow higher metal loading have higher electrical resistivity. Sheet resistivity versus metal loading for screened metallization is given in Table 3.

Table 3 – Sheet Resistivity vs Loading for Screened Metallization

<table>
<thead>
<tr>
<th>Layer Metal Loading (Area %)</th>
<th>Sheet Resistivity (mΩ/square)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 – 70 I</td>
<td>40</td>
</tr>
<tr>
<td>20 – 50</td>
<td>17</td>
</tr>
<tr>
<td>&lt;20</td>
<td>10</td>
</tr>
</tbody>
</table>

Loading in this range requires approval from Technical Support.

2.2.2.1 Transverse Loading

Always attempt to design metal patterns that:

- Minimize the total metallization area on each layer
- Are symmetrical about the center of the part
- Do not create localized regions of high loading

To calculate a layer loading metric, use the following equation. Limits on loading are described in Table 2.

\[
\text{Percent Layer Metal Loading} = \frac{\text{(Total area covered by features)}}{\text{(Total Substrate Area) - (Cavity Area)}} \times 100\%
\]

The "Total area covered by features" refers to the sum of the areas covered by each individual metallization feature (i.e., not the same thing as the active area).

Note that Cavity Area is only meaningful in cavity substrates. In non-cavity substrates, Cavity Area = 0.
2.2.2.2 Z-Loading (Top to Bottom)

Balancing Z>Loading is also important to improving manufacturability. Avoid abrupt changes in Z-Loading, except where required as in cases of Power Distribution planes. The ideal design would have the amount of metal above the substrate center-line equal to the amount below, with gradual changes in loading between neighboring layers. In practice, some variation in Z-Loading is tolerable.

2.3 General Ceramic and Metallization Rules

Tables 4 and 5 summarize the general design rules applicable to co-fired AlN multi-layer ceramic products.

Table 4 – Co-fired AlN Multi-layer Ceramic General Rules

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Standard</th>
<th>Enhanced</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Co-fired Ceramic Feature Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8Body Size</td>
<td>Maximum</td>
<td>89 square</td>
<td>127 square</td>
<td>mm</td>
</tr>
<tr>
<td>8Body Size Tolerance, As-fired</td>
<td>Maximum</td>
<td>+1-1%</td>
<td>+1-0.5%</td>
<td>-</td>
</tr>
<tr>
<td>Camber, As-fired</td>
<td>Maximum</td>
<td>40</td>
<td>Same</td>
<td>.1mm/m</td>
</tr>
<tr>
<td>Camber, Lapped</td>
<td>Maximum</td>
<td>10</td>
<td>0.7</td>
<td>.1mm/m</td>
</tr>
<tr>
<td>Surface Finish: As-fired</td>
<td>Maximum</td>
<td>1.00</td>
<td>Same</td>
<td>.1mm/m</td>
</tr>
<tr>
<td>Lapped Polished</td>
<td>Maximum</td>
<td>0.75</td>
<td>Same</td>
<td>.1mm/m</td>
</tr>
<tr>
<td>8Body Thickness, As-fired</td>
<td>Minimum</td>
<td>0.64</td>
<td>Same</td>
<td>mm</td>
</tr>
<tr>
<td>8Body Thickness Tolerance, As-fired</td>
<td>Maximum</td>
<td>+1-10%</td>
<td>Same</td>
<td>-</td>
</tr>
<tr>
<td>8Body Thickness Tolerance, Lapped</td>
<td>Maximum</td>
<td>+1-0.076</td>
<td>0.025</td>
<td>mm</td>
</tr>
</tbody>
</table>

Co-fired Metal Feature Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Standard</th>
<th>Enhanced</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line or Feature Dimensional Tolerance</td>
<td>Maximum</td>
<td>+1-0.025</td>
<td>Same</td>
<td>mm</td>
</tr>
<tr>
<td>Via Pitch</td>
<td>Minimum</td>
<td>3x(via diameter)</td>
<td>2x(via diameter)</td>
<td>-</td>
</tr>
<tr>
<td>Via Perimeter to Cavity Edge Spacing</td>
<td>Minimum</td>
<td>0.64</td>
<td>Same</td>
<td>mm</td>
</tr>
<tr>
<td>Via Perimeter to Substrate Edge Spacing</td>
<td>Minimum</td>
<td>1.00</td>
<td>0.75</td>
<td>mm</td>
</tr>
<tr>
<td>Metal Feature to Cavity Edge Spacing</td>
<td>Minimum</td>
<td>0.64</td>
<td>Same</td>
<td>mm</td>
</tr>
<tr>
<td>Metal Feature to Substrate Edge Spacing</td>
<td>Minimum</td>
<td>0.75</td>
<td>0.64</td>
<td>mm</td>
</tr>
</tbody>
</table>

The flatness at the perimeter of cavity bottoms cannot be held to this value. Contact Technical Support for details.

Contact Technical Support to discuss thinner substrates.
Co-fired AIN Design Rules

Table 5 – Global Spacing, Via Sizes, and Line Widths

<table>
<thead>
<tr>
<th>Ceramic Layer Thickness Options</th>
<th>Via Hole Diameter Options</th>
<th>Via Cap Diameter (mm)</th>
<th>(Trace) Line Width</th>
<th>Minimum Spacing Edge-to-Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Trace-to-Feature</td>
<td>Cap-to-Cap</td>
</tr>
<tr>
<td>Standard Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.127</td>
<td>0.11</td>
<td>0.150</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td>0.127</td>
<td>0.12</td>
<td>0.178</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td>Enhanced Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.179</td>
<td>0.11</td>
<td>0.150</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td>0.179</td>
<td>0.12</td>
<td>0.178</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td>0.179</td>
<td>0.17</td>
<td>0.250</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td>0.267</td>
<td>0.17</td>
<td>0.250</td>
<td>0.150</td>
<td>0.150</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1Do not mix via hole diameters on a single ceramic layer. Exception: Wire bond layers for small pads when necessary. Consult with Technical Support for special considerations when you do this.
2Preferred combination of layer thickness and via hole diameter
3Via Cap sizes are minimum values; larger is acceptable, but minimize the number of circle sizes used per the Layout Rules for Aluminum Nitride Design.
4Use of Enhanced Ground Rules will have impact on cost that is a function of the extent to which they are used.

2.4 Via Columns

A "Via Column" is a column of metal created by the existence of vias at the same (X,Y) location in contiguous substrate Via Layers.

In general, it is not recommended that a via column extend completely through a substrate (from the top to bottom surfaces).

Via column length can be controlled by jogging the via away from the original location by at least one via diameter after passing through a certain number of layers. After this initial jog, it is acceptable to jog back to the original position after passing through the next layer. (When making short jogs, observe the rule described in Layout Rules for Aluminum Nitride Design, "Figure Eights").

Contact Technical Support (Section 1.1) about designs with via columns near chip connection pads or extending completely through the substrate.
2.5 Large Solid Features

Special considerations must be made when designing large solid features (i.e., relatively large areas of unbroken metallization). These features often include Power Distribution planes, die attach pads, and other large rectangles and circles.

Definition of Large Solid Feature: Any feature that is larger than 2.125 mm in both the X and Y directions is termed a Large Solid Feature. Such Large Solid Features can be inadvertently created by combining several other features. When this happens on a square hatch Reference Layer, you do not have the option of doing the procedure that follows (See "Square Hatch" section in Layout Rules for Aluminum Nitride Designs). On Reference of Mixed Layers, Large Solid Features must be eliminated by rearranging the locations of Fill Lines.

What to Do:

- Place perforations at least every 1 mm. A perforation is an area where conductor metal is omitted. They are typically designed as a square 0.25 mm on a side. See Figure 2.1 for an example. (This does not apply to seal bands or BSM pads.)

Figure 2.1 – Example of Perforation Design for Large Solid Features
2.6 Things to Avoid

Avoid or minimize the occurrence of the following design and layout conditions:

• Mixing grids – Use a single Design Grid throughout all portions and layers of a design. Likewise, use a single via grid to the extent possible. Some features (e.g., wire bond pads) will force additional via grids on certain layers.

• Risk Sites (Figure 2.2) – Avoid minimum spacings and featured whenever possible.

• Using Mixed Layers – Use separate signal and reference layers as much as possible.

Figure 2.2 – Examples of Risk Sites
3.0 Design Rules by Layer Type

3.1 Redistribution Layer Rules

A Redistribution Layer is a metallization layer (in a ceramic substrate) that implements the interconnections from chip bond pads to some feature on a Design Grid point as illustrated in Figure 3.1. For an MCM, the grid location will typically be a via located on the basic via grid. For an SCM the grid location may be an I10 site. Rules specific to Redistribution Layers are in Table 5.

See Layout Rules for Aluminum Nitride Designs for feature construction rules applicable to Redistribution Layers. A few points worth noting here are:

Tapered Lines: Do not use tapered lines if it is possible to avoid them. The preferred method for changing widths is to end the line of one width and start a line with the new width. See Layout Rules for Aluminum Nitride Designs for information on creating tapered lines if they must be used to implement a design.

Figure 3.1 - Redistribution Layer Example

<table>
<thead>
<tr>
<th>Rule Descriptions</th>
<th>Recommended/Standard</th>
<th>Enhanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>Space from edge-of-substrate to edge-of-metal, minimum</td>
<td>See Global Rules</td>
<td>See Global Rules</td>
</tr>
<tr>
<td>Preferred line orientations</td>
<td>0, 45, 90</td>
<td>0, 45, 90</td>
</tr>
</tbody>
</table>
3.2 Signal (X-Y) Layer Rules

This section describes the rules for a disciplined design methodology for implementing signal traces that makes use of a rigid Design Grid. It is not necessary to strictly follow these rules in designs using screened metallization. Mixed Layer and Redistribution Layer rules may be applied instead. However, aspects of the methodology may be of benefit to any design. Reading and consideration of these rules are recommended.

In many multi-chip modules, chip-to-chip and chip-to-I/O wiring is placed on signal layers that are separate from Redistribution, Reference, or Power Distribution Layers. For electrical reasons, X-Y type wiring may be employed on an SCM also, even though no chip-to-chip wiring is present. All design rules governing Signal Layer wiring for MCM would be observed in that event. Signal Layer wiring is done utilizing two layer sets (or "plane-pairs") where horizontal wiring is exclusively done on one set (or "X") layers and vertical wiring is done on the other set (or "Y") layers. The horizontal and vertical wiring is connected in the Z direction between the plane-pair layers through the use of vias. Multiple sets of plane-pairs may be employed for extensive wiring demand. A portion of a Signal Layer is illustrated in Figure 3.2.

There are certain considerations unique to Signal Layers:

- A series of Design Grid points for both vias and trace (line) channels must be established for these layers. These grid points should preferably be represented by a 0.50 mm X and Y pattern, or in the case of an enhanced design, on a multiple of the substrate Design Grid (minimum is 0.45 mm). For ease of design, the grid is often a multiple of the top surface grid (which is driven by Chip I/O pitch).

- Wiring traces ("right-way" wiring) should only reside in wiring channels, and vias should only be placed on the via grid. The only exception is the short interconnections between traces and vias. These short connecting traces are referred to as "wrong-way" wiring and are subject to the restrictions in Table 6.

- Connections between vias should always route in a designated wiring channel. Connections made in a via channel, even though very short, are not allowed (See Figure 3.2).

Table 6 – Signal Layer Rules

<table>
<thead>
<tr>
<th>Rule Descriptions (Global Layer Rules Apply)</th>
<th>Recommended/Standard</th>
<th>Enhanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = Space from edge-of-substrate to edge-of-metal, minimum</td>
<td>See Global Rules</td>
<td>See Global Rules</td>
</tr>
<tr>
<td>B = Wrong-way wiring, maximum (8max)</td>
<td>1.00 mm</td>
<td>1.00 mm</td>
</tr>
<tr>
<td>C = Via grid (Pitch), minimum</td>
<td>0.50 mm</td>
<td>0.45 mm</td>
</tr>
<tr>
<td>D = Wiring Channel grid (Pitch), minimum</td>
<td>0.50 mm</td>
<td>0.45 mm</td>
</tr>
<tr>
<td>Trace orientations</td>
<td>0, 90</td>
<td>0, 90</td>
</tr>
<tr>
<td>Trace intersection angles</td>
<td>90, 180</td>
<td>90, 180</td>
</tr>
</tbody>
</table>

* Any multiple of the overall substrate design grid with a minimum of 0.45 mm is acceptable. The via grid and wiring channel pitch must be the same.
Figure 3.2 – Signal Layer Example  Note that there are multiple examples of dimension 8 (wrong-way wiring), but only one example of a maximum wrong-way wiring (8max)

3.3 Mixed Layer Rules

To enhance manufacturability, it is recommended that designs be implemented using separate metallization layers for Signal or Redistribution functions and Reference or Power Distribution functions. However, it is recognized that some product designs, such as certain RF or microwave modules, may require that signal and reference metallization be present on the same layer. In order to meet performance criteria, some circuits may also require curved lines or tapered lines that are discouraged in the design and layout rules. The following rules apply to Mixed Layers:

- Follow all design rules for Signal and Reference Layers to the extent that is possible. In particular, apply grid rules as much as possible. Apply rules for Redistribution and Power Distribution Layers as required.
- Pay attention to the impact that mixing layer types within layers has on metal loading and balancing.
- Limit signal routing to either "X" or "Y" routing as much as possible.
- Limit the use of curved and tapered features. See Layout Rules for Aluminum Nitride Designs for how to implement approximations of such features.
3.4 Reference and Power Distribution Layer Rules

Reference planes are layers of metal placed between wiring layers (Redistribution, Signal, or Mixed Layers) for noise decoupling and impedance control. They are typically designed as full dense square hatch (sometimes half-dense square hatch) patterns where the pitch (grid) of the design is consistent with the pitch (grid) of the wiring layer. Reference planes are electrically connected to Power Distribution planes in the substrate.

Power Distribution planes (power planes for short) are layers of metal used in the substrate to distribute current and voltage from the I/O pins (S8C, leads, etc.) to chip power and ground terminals. Power planes may be designed with limited solid regions, but it is preferred that they be designed as square hatch planes.

See Layout Rules for Aluminum Nitride Designs for details of how to implement the geometric features used to construct Reference and Power Distribution Layers. In general, half-dense square hatch patterns are preferred over full-dense square hatch patterns in order to limit metal loading. See Section 3.4.3 for more information on Square Hatch designs.

3.4.1 Reference Layer Rules

The rules for Reference Layer features are given in Table 7 and illustrated in Figure 3.3. Regions of solid metallization can be created on Reference Planes using a number of neighboring Fill Lines. It is strongly suggested that the use of such regions be minimized with careful consideration given to the impact on metal loading and balancing. See Section 2.5, “Large Solid Features”, for related information.

Figure 3.3 - Reference Layer Example (Full-Dense Square Hatch)
Table 7 – Reference Layer Rules

<table>
<thead>
<tr>
<th>Layer Rule Descriptions (Global Rules Apply)</th>
<th>Recommended/Standard</th>
<th>Enhanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>Space from edge-of-substrate to edge-of-metal, minimum</td>
<td>See Global Rules</td>
<td>See Global Rules</td>
</tr>
<tr>
<td>Grid Options - FDSQ - HDSH</td>
<td>≥0.50 mm</td>
<td>≥0.45 mm</td>
</tr>
<tr>
<td></td>
<td>≥1.00 mm</td>
<td>≥0.90 mm</td>
</tr>
<tr>
<td>Line Orientations</td>
<td>0, 90</td>
<td>0, 90</td>
</tr>
<tr>
<td>Line intersection angles</td>
<td>90, 180</td>
<td>90, 180</td>
</tr>
</tbody>
</table>

3.4.2 Power Distribution Layer Rules

Power Distribution planes are used in a substrate design where large areas of metallization are required to evenly distribute a voltage potential. Several rules are summarized below, particularly in Figure 3.4 and Table 8. It is strongly recommended that nominally solid power planes be perforated with small openings if the design allows. See Figure 3.4 for an illustration. Square openings that are 0.25 mm on a side placed on a 1.0 mm pitch are recommended.

Via Clearances: Clearances must be provided for through vias that are not supposed to contact the power plane. Individual via clearances must be square. Via clearances may overlap to create clearance regions that are not square but do have orthogonal sides. Whenever non-square clearance regions are created, the region must be outlined with border lines of an appropriate width. See Layout Rules for Aluminum Nitride Designs for more details on implementing non-square clearance regions.

Table 8 – Power Distribution Layer Rules

<table>
<thead>
<tr>
<th>Rule Description</th>
<th>Recommended/Standard</th>
<th>Enhanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = Space: Via Cap-to-Plane, minimum</td>
<td>0.175 mm</td>
<td>0.175 mm</td>
</tr>
<tr>
<td>8 = Plane Feature Width, minimum</td>
<td>0.30 mm</td>
<td>0.30 mm</td>
</tr>
<tr>
<td>C = Via Clearance Width, minimum</td>
<td>(Via Cap Diam) + 2A</td>
<td>(Via Cap Diam) + 2A</td>
</tr>
<tr>
<td>D = Space: Feature to edge-of-substrate, minimum</td>
<td>1.50 mm</td>
<td>1.50 mm</td>
</tr>
<tr>
<td>E = Space: Net to edge-of-metal, minimum</td>
<td>0.175 mm</td>
<td>0.175 mm</td>
</tr>
<tr>
<td>F = Space: Net to Voltage Line, minimum</td>
<td>Maximize</td>
<td>See Global Rules</td>
</tr>
<tr>
<td>G = Space: Net Cap to Plane Cap, minimum</td>
<td>Maximize</td>
<td>See Global Rules</td>
</tr>
<tr>
<td>H = Voltage Line Width</td>
<td>See Global Rules</td>
<td>See Global Rules</td>
</tr>
</tbody>
</table>
3.4.3 Square Hatch

Square hatch designs, such as the samples shown in Figure 3.5, achieve their power distribution and shielding by using a grid of lines (i.e., a mesh) instead of a solid plane. Vias pass through the hatch in open areas. Vias connect to the plane by means of a fill (See Layout Rules for Aluminum Nitride Designs for rules on implementing hatch patterns and fills.) The grid must be chosen to be consistent with the chosen via grid.

Full-Dense Square Hatch (FDSH): This refers to a design method for creating Reference Planes. An example appears in Figure 3.5.

Typically, Reference Planes are designed following a 0.5 mm grid system in which there is a line making up the elements of the Reference Plane every 0.5 mm.

Half-Dense Square Hatch (HDSH): Whenever possible, use half-dense square hatch designs instead of full-dense designs to limit metal loading. Typically, a 1.0 mm grid system is used instead of a 0.5 mm, but again the via grid must be considered. See Figure 3.5 for an example.
3.5 Capacitor Layers

Capacitor Layers are buried ceramic layers that are thinner than the standard layer thickness offerings. Capacitor Layers are not currently offered in the Aluminum Nitride technology. Consult with Technical Support (Section 1.1) if you have a need for capacitor layers.

4.0 Cavities

Contact Technical Support (Section 1.1) for the design of substrates with cavities.